TENT COOPERATION TRE

From the INTERNATIONAL BUREAU

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NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

United States Patent and Trademark Office
(Box PCT)
Crystal Plaza 2
Washington, DC 20231
ÉTATS-UNIS D'AMÉRIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 14 June 1999 (14.06.99)	
International application No. PCT/GB98/03142	**Applicant's or agent's file reference** DWS/VV/P227WO
International filing date (day/month/year) 22 October 1998 (22.10.98)	**Priority date** (day/month/year) 22 October 1997 (22.10.97)
Applicant TUCK, Richard, Allan et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

14 May 1999 (14.05.99)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland** Facsimile No.: (41-22) 740.14.35	Authorized officer C. Carrié Telephone No.: (41-22) 338.83.38

PATENT COOPERATION TREATY

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INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference DWS/VV/P227WO	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
International application No. PCT/GB 98/03142	International filing date *(day/month/year)* 22/10/1998	(Earliest) Priority Date *(day/month/year)* 22/10/1997
Applicant PRINTABLE FIELD EMITTERS LTD. et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. [ ] **Certain claims were found unsearchable** (see Box I).

2. [ ] **Unity of invention is lacking** (see Box II).

3. [ ] The international application contains disclosure of a **nucleotide and/or amino acid sequence listing** and the international search was carried out on the basis of the sequence listing
   - [ ] filed with the international application.
   - [ ] furnished by the applicant separately from the international application,
     - [ ] but not accompanied by a statement to the effect that it did not include matter going beyond the disclosure in the international application as filed.
   - [ ] Transcribed by this Authority

4. With regard to the **title**,
   - [X] the text is approved as submitted by the applicant
   - [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   - [X] the text is approved as submitted by the applicant
   - [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this International Search Report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is:

   Figure No. 3
   - [X] as suggested by the applicant.
   - [ ] because the applicant failed to suggest a figure.
   - [ ] because this figure better characterizes the invention.
   - [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
/GB 98/03142

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01J9/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 795 622 A (MOTOROLA INC) 17 September 1997 see figures 9-11 see column 11, line 13 - line 17 see column 14, line 13 - line 53 ---	1,11
Y	HOOLE A C F ET AL: "DIRECTLY PATTERNED LOW VOLTAGE PLANAR TUNGSTEN LATERAL FIELD EMISSION STRUCTURES" JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART B, vol. 11, no. 6, 1 November 1993, pages 2574-2578, XP000423379 see page 2574, column 2, paragraph 4 - page 2575, column 2, paragraph 1 see figure 2 --- -/--	1,11

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 January 1999	28/01/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Noordman, F

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Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 685 869 A (MOTOROLA INC) 6 December 1995 see column 1, line 18 - line 22 see column 6, line 50 - column 7, line 26; figure 6 ---	1,11
A	WO 97 06549 A (TUCK RICHARD ALLAN ;LATHAM RODNEY VAUGHAN (GB); TAYLOR WILLIAM (GB) 20 February 1997 cited in the application see page 24, line 12 - page 25, line 18; figure 13 -----	1

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 98/03142

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0795622 A	17-09-1997	US 5837331 A	17-11-1998
		JP 9245626 A	19-09-1997
EP 0685869 A	06-12-1995	US 5473218 A	05-12-1995
		JP 8055564 A	27-02-1996
WO 9706549 A	20-02-1997	AU 6626096 A	05-03-1997
		CN 1192288 A	02-09-1998
		EP 0842526 A	20-05-1998
		GB 2304989 A,B	26-03-1997
		GB 2306246 A,B	30-04-1997

M.H

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PATENT COOPERATION TREATY

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REC'D 04 FEB 2000
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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference DWS/VV/P227WO	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/GB98/03142	International filing date *(day/month/year)* 22/10/1998	Priority date *(day/month/year)* 22/10/1997
International Patent Classification (IPC) or national classification and IPC H01J9/02		
Applicant PRINTABLE FIELD EMITTERS LTD. et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 27 sheets.

3. This report contains indications relating to the following items:

   I ☒ Basis of the report
   II ☐ Priority
   III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   IV ☐ Lack of unity of invention
   V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   VI ☐ Certain documents cited
   VII ☐ Certain defects in the international application
   VIII ☒ Certain observations on the international application

Date of submission of the demand 14/05/1999	Date of completion of this report 01.02.00
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Frank, V Telephone No. +49 89 2399 2726

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB98/03142

I. Basis of the report

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

Description, pages:

2,3	as originally filed			
1,4-26	as received on	14/01/2000	with letter of	05/01/2000

Claims, No.:

1-15	as received on	14/01/2000	with letter of	05/01/2000

Drawings, sheets:

1/13-13/13	as originally filed

2. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-15
	No:	Claims	
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-15
Industrial applicability (IA)	Yes:	Claims	1-15
	No:	Claims	

2. Citations and explanations

see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item V

Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Reference is made to the following documents:

D1: EP-A-0 795 622

D2: HOOLE A C F ET AL: 'DIRECTLY PATTERNED LOW VOLTAGE PLANAR TUNGSTEN LATERAL FIELD EMISSION STRUCTURES' JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART B, vol. 11, no. 6, 1 November 1993, pages 2574-2578

1. Document D1 discloses a manufacturing method of a field emission device from which the subject-matter of claim 1 differs in that
i) the cathode electrode and the gate electrode are formed by low resolution means (steps a and b),
ii) a photoresist layer is formed over this structure (step c),
iii) the emitting cells are formed by exposing said photoresist layer by high resolution means (step d) and
iv) the remaining photoresist is removed.

It is obvious to a skilled person that the formation of the emitter well 712 in D1 (cf. Fig. 11 and the corresponding text) comprises the features ii) to iv) mentioned above, although they are not specifically disclosed in this document.

The problem to be solved by the present invention may therefore be regarded as the reduction of manufacturing costs of such a device, having regard to feature i) mentioned above. The posing of this problem does not involve an inventive step, since it is one of the constant objects of the skilled person to reduce the manufacturing cost of a given device.

Document **D2** discloses (cf. page 2574, "III. Device Fabrication") a fabrication method of a field electron emission device in which the probe circuitry and the necessary alignment marks are exposed by low resolution e-beam exposure (cf. Fig. 2a) and the required finer patterns are written by high resolution e-beam

exposure (cf. Fig. 2b).

The subject-matter of claim 1 lacks thus an inventive step over the combination D1/D2, as the concept of using low and high resolution exposure means as required is clearly taught by D2.

2. Dependent claims 2-15 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of inventive step, since they comprise only features that are known from the prior art.

Re Item VIII
Certain observations on the international application

1. The relative terms "low resolution means" and "high resolution means" used in **claim 1** have no well-recognised meaning and leave the reader in doubt as to the meaning of the technical features to which they refer, thereby rendering the definition of the subject-matter of said claim unclear (PCT/GL/3-4.5).

2. Claim 6 is not supported by the description as required by Article 6 PCT, as its scope is broader than justified by the description and drawings. The reasons therefor are the following: claim 6 defines the conducting layer formation step by a negative statement, i.e. excluding two deposition methods. However, a claim should be defined by positive features, i.e. the specific deposition methods disclosed in the application.

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WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01J 9/02

A1

(11) International Publication Number: WO 99/21207

(43) International Publication Date: 29 April 1999 (29.04.99)

(21) International Application Number: PCT/GB98/03142

(22) International Filing Date: 22 October 1998 (22.10.98)

(30) Priority Data:
9722258.2 22 October 1997 (22.10.97) GB

22 Apr 00 / 30 mon

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(71) Applicant (*for all designated States except US*): PRINTABLE FIELD EMITTERS LTD. [GB/GB]; 6 Elm Grove, Hartlepool TS26 8LZ (GB).

(72) Inventors; and
(75) Inventors/Applicants (*for US only*): TUCK, Richard, Allan [GB/GB]; 34 Park Lane, Slough SL3 7PF (GB). JONES, Peter, Graham, Adpar [GB/GB]; 56 King's Ride, Penn, High Wycombe HP10 8BP (GB).

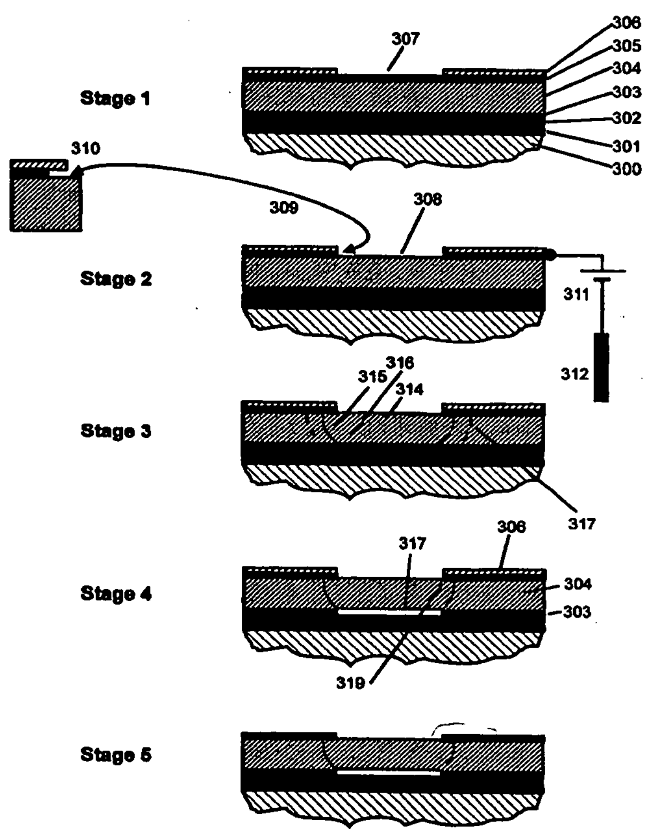
(74) Agent: STANLEY, David, William; Kings Court, 12 King Street, Leeds LS1 2HL (GB).

Published
With international search report.

(54) Title: FIELD EMISSION DEVICES

(57) Abstract

A field electron emission cathode is manufactured by depositing on an insulating substrate (300), by low resolution means, a sequence of a first conducting layer (301), a field emitting layer (302) and a second conducting layer (303) to form at least one cathode electrode. There is then deposited on the cathode electrode by low resolution means, a sequence of an insulating layer (304) and a third conducting layer (305), to form at least one gate electrode. The structure thus formed is then coated with a photoresist layer (306). The photoresist layer (306) is then exposed by high resolution means to form at least one group of emitting cells, the or each such group being located in an area of overlap between a cathode electrode and gate electrode. To complete the cells, the conducting and insulating layers (305, 304, 303) are etched sequentially to expose the field emitting layer (302) in the cells, and remaining areas of the photoresist layer (306) are removed. Thus, field emitting materials and devices can be manufactured using relatively low cost techniques.



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FIELD EMISSION DEVICES

This invention relates to field emission devices and in particular to methods of manufacturing addressable field electron emission cathode arrays. Preferred embodiments of the present invention aim to provide low manufacturing cost methods of fabricating multi-electrode control and focusing structures.

It has become clear to those skilled in the art that the keys to practical field emission devices, particularly displays, are arrangements that permit the control of the emitted current with low voltages. The majority of the art in this field relates to tip-based emitters - that is, structures that utilise atomically sharp micro-tips as the field emitting source.

There is considerable prior art relating to tip-based emitters. The main objective of workers in the art has been to place an electrode with an aperture (the gate) less than 1 μm away from each single emitting tip, so that the required high fields can by achieved using applied potentials of 100V or less - these emitters are termed gated arrays. The first practical realisation of this was described by C A Spindt, working at Stanford Research Institute in California *(J.Appl.Phys. 39,7, pp3504-3505, (1968))*. Spindt's arrays used molybdenum emitting tips which were produced, using a self masking technique, by vacuum evaporation of metal into cylindrical depressions in a SiO_2 layer on a Si substrate. Many variants and improvements on the basic Spindt technology are described in the scientific and patent literature.

An alternative important approach is the creation of gated arrays using silicon micro-engineering. Field electron emission displays utilising this

Preferred embodiments of the present invention aim to provide cost-effective field emitting structures and devices that utilise broad-area emitters. The emitter structures may be used in devices that include: field electron emission display panels; high power pulse devices such as electron MASERS and gyrotrons; crossed-field microwave tubes such as CFAs; linear beam tubes such as klystrons; flash x-ray tubes; triggered spark gaps and related devices; broad area x-ray sources for sterilisation; vacuum gauges; ion thrusters for space vehicles; particle accelerators; lamps; ozonisers; and plasma reactors.

According to one aspect of the present invention, there is provided a method of manufacturing a field electron emission cathode, comprising the steps of:

a. depositing on an insulating substrate by low resolution means, a sequence of a first conducting layer, a field emitting layer and a second conducting layer to form at least one cathode electrode;

b. depositing on said cathode electrode by low resolution means, a sequence of an insulating layer and a third conducting layer, to form at least one gate electrode;

c. coating the structure thus formed with a photoresist layer;

d. exposing said photoresist layer by high resolution means to form at least one group of emitting cells, the or each said group being located in an area of overlap between one said cathode electrode and one said gate electrode;

e. etching sequentially said conducting and insulating layers to expose said field emitting layer in said cells; and

f. removing remaining areas of said photoresist layer.

Preferably, said cathode is a cathode array, said cathode electrode and said gate electrode comprise respectively cathode addressing tracks and gate addressing tracks, which tracks are arranged in addressable rows and columns, and step d. includes forming a pattern of said groups of emitting cells.

Preferably, at least one of or all of said cathode addressing tracks address(es) a plurality of rows or columns of cells.

Each row and/or column can be thin or wide, to take in as few or as many cells as desired, depending upon the application of the cathode.

Preferably, said steps of exposing and etching include the formation of fiducial marks on the cathode array, to facilitate the subsequent alignment of the array with an anode or other component after manufacture of the array.

A method as above may comprise the step of forming at least one of said conducting layers by application of a liquid bright metal or by electroless plating.

A method as above may comprise the step of forming at least one of said conducting layers by a means other than vacuum evaporation or sputtering.

Preferably, said field emitting layer comprises a layer of broad area field emitter material.

A method as above may comprise the further steps of depositing sequentially a second insulating layer and fourth conducting layer onto the cathode after completion of steps a. to f., to form a focus grid.

The invention extends to a field electron emission cathode which has been manufactured by a method according to any of the preceding aspects of the invention.

According to another aspect of the present invention, there is provided a field emission device comprising an anode having electroluminescent phosphors and a cathode as above, wherein the cathode is a cathode array as above and is arranged to bombard said phosphors.

Preferably, said phosphors are arranged in groups of red, green and blue to form a colour display.

A field emission device as above may include anode driving means for energising said red, green and blue groups in turn.

A field emission device as above may further comprise an electrode of interdigitate or mesh form which is interposed between said phosphors and is arranged to be driven at a potential less than that at which said phosphors are driven, thereby to form potential wells around the phosphors in order to attract electrons towards said phosphors and compensate for any misalignment between cathode and anode.

The cathode may be provided with a further control grid over said gate electrode, and a driving means for so driving said control grid as to retard electrons emitted by the cathode.

Such a field emission device may further comprise means for providing a magnetic field normal to the emitter surface.

The first conducting layer, field emitting layer and second conducting layer may be patterned using low resolution means, as a whole or on a layer by layer basis. The same applies to the insulating layer and third conducting layer. The high resolution exposure step is preferably the only high resolution step required in the whole manufacturing method, and is such that the tolerance on location of the groups, with respect to the intersections of the tracks, is determined by the relatively large track (eg row and column) dimensions rather than the much smaller emitter cell dimension. A first etch for the conducting layers is preferably chosen such that it does not attack the insulating or field emitting layers. A second etch for the insulating layers is preferably chosen such that it does not attack the conducting layers. Thus, the etching can be being carried out in sequential steps using the first and second etches alternately, such that each layer after etching forms a mask for the next layer to be etched, thereby providing self-alignment of the apertures in the layers.

In the context of this specification, the meaning of "low resolution means" and "high resolution means" is as follows. The high resolution means is a means capable of forming well-defined structures of the chosen emitter cell size. The low resolution means is a means capable of forming well-defined structures of the chosen size of cathode addressing tracks but not of the smaller, chosen emitter cell size.

For example, the high resolution means may be a means capable of forming well-defined structures of a minimum size which is equal to or

smaller than 50%, 40%, 30%, 20%, 10% or 5% of the minimum size of well-defined structure that can be formed by the low resolution means. The low resolution means may be a lithographic means that can form well-defined structures down to a minimum dimension of 100, 70, 50, 40 or 30 μm. The high resolution means may be a photo-etching means that can form well-defined structures down to a minimum dimension of 20 or 10 μm or less, and preferably down to a few μm across or less. As one example, cathode and gate tracks 100 μm across are formed by lithography means, and emitter cells 8 μm across are formed by photo-etching means.

For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1a shows four pixels of an addressable array as would be used in a large area monochrome field emission display;

Figure 1b shows an idealised emitter cell structure;

Figure 1c illustrates the problems of realising such a structure using thick film fabrication techniques;

Figure 1d shows how a near-ideal emitter cell structure may be fabricated using liquid bright gold and a glaze;

Figure 1e shows how the structure in Figure 1d may be improved by the use of a planarising layer between an insulator and final conducting layer;

Figure 2 shows a pixel arrangement in a colour display;

Figure 3 shows etch steps in forming an emitting cell;

Figures 4 (a) to (f) show steps in forming an addressable array using photolithography;

Figures 5 (a) to (d) shows steps in forming an addressable array using a mixture of printing and photolithography;

Figures 6 (a) and (b) show how focusing electrodes may be incorporated into devices;

Figure 7 illustrates a complete display using methods and structures described herein; and

Figures 8 (a) and (b) show how misalignment between emitter cell groups and phosphor patches on an anode may be accommodated by special anode structures.

Embodiments of this invention may have many applications and will be described by way of the following examples. It should be understood that the following descriptions are only illustrative of certain embodiments of the invention. Various alternatives and modifications can devised by those skilled in the art.

In large field emitting displays the pixel dimensions are well within the capabilities of a number of low cost patterning techniques such as screen

printing or photo-etching. For example printed circuits can now be made with well defined 75 μm tracks.

Figure 1a shows four pixels in a hypothetical 16:9 HDTV display (monochrome for simplicity) with a diagonal dimension of one metre. Dimension 131 is 0.75 mm and dimension 130 is 0.50 mm. Figure 2 shows two pixels of a similar colour display where dimensions 234 and 235 correspond with dimensions 131 and 130 in Figure 1a. Columns 231,232 and 233 control current flow to phosphors in the three primary colours.

Referring again to Figure 1a, it can be seen that cathode address rows 112 and gate address columns 122 are some tenths of a millimetre wide and capable of being formed by a range of printing and lithographic techniques. However, the emitter cell dimensions 120 are dictated by the transconductance required to achieve the desired control voltage. Because of the large number of channels, the drive electronics form a major cost element in any matrix addressed display, with higher voltage devices costing proportionally more. To achieve overall acceptable costs the drive voltages are preferably a few tens of volts.

With reference to Figure 1a, the emitter cells may be arrays of, for example, slotted 120 or circular forms 121. Figure 1b shows a section across the narrow dimension of two such emitter cells. The structure is formed on an insulating substrate 111. The layers are as follows: cathode address rows 112; a field emitter material 113; shadow grid layer 114; gate (grid) insulator layer 115; grid address columns 116.

For electron optical reasons dimensions 118 and 119 must be comparable with each other. Such an arrangement also facilitates easy

etching. Electrostatic modelling shows that for a 40V control voltage swing (negative-going on the rows and positive-going on the columns) dimension 118 is approximately 8 μm. For a 15V swing it reduces to approximately 4 μm.

Whilst these dimensions are small, it has occurred to us that, with a suitable self-aligning process, single exposures of resist patterns to create them fall within the regime of one to one contact exposure or one to one proximity exposure with collimated illumination. Suitable large area high intensity exposure systems, both with and without collimation, are manufactured for printed circuit board fabrication. It is only if multiple exposures are required that the very expensive and slow stepping and alignment equipment that characterises semiconductor manufacture is required. Furthermore, the location of each emitter group within the pixel region may be subject to a much larger tolerance (position 141 to 140) than that required if multiple mask steps were required to form the emitter cells.

To enable the above emitter patches to be aligned with the phosphor pattern on the anode during the assembly of the display panel, fiducial marks in known positions relative to the pattern of emitter cells may be photo-etched during the single high resolution mask stage.

Given that the row and column structures are of a size capable of being screen printed one might be tempted to consider using standard electronic thick film circuit pastes to form the structures. Figure 1c illustrates the problem with this approach where the goal is a structure as in Figure 1b with dimension 118 of approximately 8 μm and dimension 119 approximately 5 μm. Conducting thick film pastes are made from metallic particles and a

glass fritt in an appropriate vehicle. Minimum layer thicknesses are around 5 μm with roughness of ±1 to 2 μm. Proprietary insulating pastes have similar roughness.

It can be seen that, even without any undercutting that may occur during etching, the structures formed by standard thick film techniques are a very poor representation of the ideal structure in Figure 1b. Not only would there be excessive variability from cell to cell but the extra depth 146 compared with the diameter 145 would be electronoptically unacceptable.

Inspection of Figure 1c shows that excessive thickness and much of the irregularity in the layers is caused by those formed from conducting pastes 142. For this reason the vast majority of field emission device fabrication processes use vacuum or plasma deposited thin films that closely conform to the profile of the substrate. Their use within examples of this invention is not precluded. However, the deposition of such films requires expensive equipment especially at large substrate sizes and high throughputs: consequently maximum reductions in manufacturing cost may only be realised using deposition techniques that do not require vacuum systems.

In a number of unrelated industries, specularly reflecting films have been produced by chemical techniques, with a good example being the silvering on mirrors. In the architectural glass industry, infrared reflecting coatings, which were produced by sputter coating, are now made by the much lower cost in situ spray pyrolysis of tin oxide films directly onto hot float glass.

For many years, the pottery and glass industries have decorated their wares with bright metallic layers using a paint that contains organometallic

compounds - the so called resinate or bright golds, palladiums and platinums. The metallic layer is formed by applying a paint and then firing the object in air at temperatures between 480°C and 920°C at which point the organometallic compound decomposes to yield pure metal films 0.1 to 0.2 μm thick. Traces of metals such as rhodium and chromium are added to control morphology and assist in adhesion. Currently most of the products and development activity concentrate on the decorative properties of the films. However, the technology is well established. Although little (or not) used, or known of, in the art today, such techniques have been used in the past by the electron tube industry. For example Fred Rosebury's classic text "Handbook of Electron Tube and Vacuum Techniques" originally published in 1964 *(Reprinted by American Institute of Physics - ISBN 1-56396-121-0)* gives a recipe for liquid bright platinum. More recently Koroda *(US Patent 4,098,939)* describes their use for the electrodes in a vacuum fluorescent display.

In critical electronic applications of liquid bright golds, care is required to avoid a bloom of sodium sulphate forming on the surface of the films. The bloom is believed to be formed by sodium compounds reacting with sulphur compounds (sulphur dioxide and/or trioxide) from the decomposition of the sulphur based gold organometallic compounds. Such bloom may be minimised or eliminated by either the use of either a low sodium glass - such as borosilicate - or by the use of coatings on sodalime glass. One suitable coating is silica deposited from a vapour phase precursor onto hot float glass. Glass treated in this way is manufactured by Pilkington under the trade name Permabloc.

Accordingly, by replacing the thick film conducting pastes with a liquid bright metal, preferably gold, one of the obstacles to a low-cost low-

voltage field emission display can be overcome. The coating formulation may be deposited by spraying, spinning, roller coating, screen printing, wire roll coating or other suitable technique and then simply fired in air. In the case of some of these techniques, for example screen printing, the formulation may be directly applied in the conducting track pattern, thus eliminating a photolithography stage.

Clearly there are other non-vacuum techniques for producing metal films. However, we are unaware of the use of any such techniques in the art of field emission devices. In part this must be due to the use of established semiconductor fabrication processes by workers who have migrated from that art. Where deviations from established techniques have taken place they are slight. For example DeMercurio et al *(US Patent 5,458,520)* uses electroplating within a gate microtip structure but only then to thicken up layers and close apertures, the initial metal layers being deposited by vacuum means.

An alternative method of forming the conducting elements is to use electroless plating with a photo-activated catalyst. There are other non-vacuum methods.

The insulating pastes used in traditional thick film technology may be replaced with a glass formulation which can be taken well past its melting point into a region where it has low viscosity and allowed to flow to a smooth film (as in a glaze) to form uniform (or near uniform) thickness gate-cathode insulator layers.

An alternative method of forming the insulating layer is by using liquid chemical precursors such as sol gels, aerogels or polysiloxanes. Once the

layer is formed it is heated to decompose the precursor to form an inorganic compound such as an oxide (e.g. Silica), a ceramic or a glass.

Figure 1d illustrates that by bringing together a low cost method of forming smooth metal layers derived from a liquid bright metal, electroless plating or other suitable process 150 and the insulator layer 151 formed from a complementary low-cost process, structures close to the ideal shown in Figure 1b may be realised.

If required, (see Figure 1e) this arrangement may be further improved by using a planarising layer 152 such as one of the spin-on glass formulations widely used in the semiconductor industry.

Example I

Referring now to Figure 3, we will describe an illustrative example. In this, emitter cells may be formed in gold/low melting point glass laminated structures on a glass substrate using wet etch processes. Naturally, dry etch processes can be used but these increase manufacturing cost.

One advantage of this combination of materials is that because low melting point glasses and gold have coefficients of thermal expansion close to that of soda lime glass, a reasonably strain free structure is produced.

Prior to stage 1, first conductive layer 301, field emitter layer 302, second conductive layer 303, insulator 304 and third, gate conductor layer 305 have been formed on substrate 300. Thus, stage 1 joins the process at a point at which all of the track patterns have been formed by low resolution patterning techniques and an appropriate photoresist layer 306 has been

exposed and developed with a pattern of grid cell apertures to expose these regions 307 of the laminate to various etch stages. A resist or lacquer will also have been applied to protect the reverse side and edges of the glass substrate.

The requirement is for two etch solutions. One solution must remove gold but not attack glass and the other remove glass but not attack gold. In this way, self-alignment of the cell structure is obtained, as will become apparent from the following description.

A suitable etch for glass that does not attack gold is hydrofluoric acid.

With etches for gold there are more options. Aqua regia, the classic gold etch, is an unpleasant material and, being strongly oxidising, may attack photoresists. Two practical formulations are a solution of iodine in potassium iodide or a solution of bromine in potassium bromide *(Bahl - US Patent 4,190,489)*.

Now, returning to Figure 3, in stage 2 the structure from stage 1 is exposed to the gold etch solution. It is known by those skilled in the art that there is a tendency for the gold to etch back under the resist as shown at 309, 310. Whilst an undersize aperture may be used to compensate for this effect during the etching of the top gold layer 305, this strategy cannot be used for layer 303. It is reported in the art *(US Patent 4,131,525)* that this undercutting is caused by electrochemical effects and can be suppressed by applying a bias voltage 311 to the gold layer relative to a platinum electrode 312 immersed in the etch solution. Once the upper gold layer has been removed to expose the glass surface 308, the assembly is rinsed to remove

any active gold etch. There will be a rinsing stage between each step but, for the sake of brevity, the rest of these are not described.

In stage 3, hydrofluoric acid is used to remove the glass gate-cathode insulating layer 304. By sloping the insulator away from the exiting electron beam, and thus reducing charging effects, any undercut 315 that occurs has a beneficial effect on the electronic performance of the emitting cell but creates some new problems at stage 4. However, it is known that the voltage-current characteristic of the structure is dominated by the size of the aperture 314. Furthermore, the arrangement of electrodes focuses the electrons as they leave the cathode, making it tolerant to an increase in the diameter of the emitter size over its nominal value which may have been caused by slight over-etching 317. In all cases the gold film 316 protects the emitter from any attack by the hydrofluoric acid and acts as an etch stop. This is particularly important with a glass-based emitter such as those described in Tuck et al *(GB Patent 2304989)*.

In stage 4 the gold etch is used to remove the layer 303, with the glass layer 304 and the resist layer 306 protecting the upper gold track 305. Erosion of the upper gold layer if it overhangs the cell 319 may be compensated for in the original size of the aperture in the resist. Again, biasing of the gold layer may be used to prevent undercutting.

In stage 5 the resist is removed to leave the completed structure.

Example II

Referring now to the various parts of Figure 4, in which views on the left hand side are cutaway plan views and views on the right hand side are

sectional views, it will be seen how the above self-aligning technique may be combined with low resolution optical lithography to produce the cathode plane of a matrix addressable field emission display. All drawings are simplified and relate to a single pixel and its associated connecting tracks.

Figure 4a shows a metal/glass-based field emitter/metal sandwich 403/402/401 deposited on a substrate 400 with an exposed and developed resist pattern defining the cathode address rows 404. For illustrative purposes the metal films are formed by a liquid bright gold process and emitter film from a fused glass-based layer *(GB 2304989)*. The precursor layers may have been deposited by spraying, spinning, silk screening, wire roll coating or some other coating technique. After coating with the formulations, each of the three layers will have been fired in air to form the final composition. In production this may be conveniently performed in tunnel furnaces.

Using the etches previously described, the gold and glass-based emitter layers are sequentially and selectively removed. Finally the resist layer is removed to form the structure 411 in Figure 4b.

Figure 4c shows the structure after it has been over-coated using the same techniques with a fusible glass insulating layer 421 and a gold gate layer 422. Again firing will have taken place in air. A resist pattern is formed to define a gate address column 423. A gold etch is used to remove the unwanted material. Finally the resist is stripped off to form the structure 431 in Figure 4d. The insulator layer 421 is left intact since the chemicals used to remove it would also attack the glass substrate.

A further layer of resist is now applied, patterned and developed using a single high resolution exposure system as previously described to form the emitter cell pattern and fiducial marks 432 shown in Figure 4e.

The emitter cell etching sequence illustrated in Figure 3 previously described as Example I is now used to form the completed structure with emitter cells 441 shown in Figure 4f.

Example III

Referring now to the various parts of Figure 5, it can be seen how the above self-aligned technique may be combined with low resolution direct printing techniques to produce the cathode plane of a matrix addressable field emission display. All drawings are simplified and relate to a single pixel and its associated connecting tracks. For ease of comparison with Example II the liquid bright gold/low melting point glass is used. However, photoactivated electroless nickel plating could be used to replace the gold with nitric acid or hydrochloric acid/ferric chloride etches. In some cases a reducing atmosphere may be used during firing operations to reduce oxidation of the nickel.

Returning now to Figure 5 we continue with the example based upon liquid bright gold and low melting point glass. Figure 5a shows substrate 511, gold 503, glass-based emitter 502, gold 501 structure formed in the same way as Example II, but in this case the precursor formulations are selectively applied, for example by screen printing, to form the desired track pattern.

Figure 5b shows a fusible glass insulator 512 and gold track 513 formed as in Example II again in the desired track pattern. If desired the insulator layer may cover the entire surface 514.

A layer of resist is now applied, patterned and developed using a single high resolution exposure system, as previously described, to form the emitter cell pattern 522 and fiducial marks 523 shown in Figure 5c.

The emitter cell etching sequence illustrated in Figure 3, previously described as Example I, is now used to form the completed structure with emitter cells 530 shown in Figure 5d.

A person skilled in the art will understand from the above teachings the significant savings in manufacturing costs that can be realised by a method which utilises a sequence of in-air processes and low-cost lithography, rather than semiconductor fabrication techniques, to form a complete field emission display cathode plane.

The use of a focus grid above a gated emitter to focus the electron beam(s) has been used and was initially described by Tuck *(US Patent 4,145,635)*. Later essentially the same arrangement was utilised in a field emitting display by Palevsky et al *(US Patent 5,543,691)*. Such a structure may be fabricated in embodiments of this invention by overlaying a further layer of insulator and a further layer of metal onto the structures of Figure 4d and 5b. Said layers may be continuous or patterned to reduce inter-track capacitance or to fulfil some other function. The emitting cells with their associated focus electrodes are then etched using the techniques previously described in Example I or, if different material systems are used, their appropriate etch systems. Figure 6a shows such a completed structure in which a substrate 600 has upon it: a cathode address layer 601; a broad area emitting layer 602; a shadow grid layer 603; a gate (grid) insulator layer 604; a control gate (grid) layer 605; a focus grid insulator layer 606 and a focus

grid 607. The anode plate 610 has upon it a transparent conducting layer 611 (for example indium tin oxide) and conducting black matrix 612 to mask the space between the cathodoluminescent phosphor patches 613. A DC potential 624 positive with respect to the ground is applied to the conducting layer 611 to accelerate the electrons from the cathode plane to energies sufficient to cause cathodoluminescence from the phosphor 613.

At the cathode plane a negative voltage 620 with respect to ground selects a cathode row, and positive voltages 621 and 612 with respect to ground modulate the current flow from the cathode. Various drive schemes may be used ranging from analogue voltage control to constant voltage pulse-width modulation. A variable voltage 623 (generally negative with respect to the control gate) forms an electron lens and focuses the beamlets.

Alternatively a much coarser focus mesh system, analogous to that described by Palevsky *(US Patent 5,543,691)*, may be fabricated by directly printing a layer of insulator and conductor onto a completed gated array. Such an arrangement is shown in Figure 6b where insulator and focus grid layers are overlaid onto a gated structure 600 identical in structure to that described earlier and illustrated in Figure 1a. Again a variable potential 604 on electrode 601 is used to focus the electron beams to strike the anode plane 603.

Moving on now to Figure 7 it can be seen how a complete field emission display may be realised that utilises the methods and structures herein described.

A cathode plane formed as described earlier 701, with or without an integral focusing grid, is joined by an hermetic seal 706 to an anode plane

702. Said anode plane 702 has upon it spacers, a conducting layer, black matrix and phosphor patches in a pixel pattern 703 as previously described. To resist the pressure of the atmosphere following evacuation spacers 704 are disposed between the pixelated structure. The spacers may be of glass, ceramic or other suitable material. The hermetic seal 706 may include a pre-formed frame and may be cemented to the cathode and anode plates with a glass fritt. During the sealing process the fiducial marks 707 (formed as previously described) are used to align the pixelated structures of the cathode and anode planes. Gettering means may be incorporated into the assembly to pump residual gasses. Some ideal locations for such getters are described by Tuck et al *(GB Patent 2,306,246)*. Evacuation and bakeout of the completed structure may be via a pumping tube and oven (not shown) or by completing the sealing process in a vacuum furnace with appropriate manipulation.

The completed display is electrically driven by a cathode addressing module 710; a column address module 711 and an anode voltage power supply 712. In the event that a focus grid is used an additional focus grid supply (not shown) is provided. Additional anode switching and focusing supplies (not shown) as later described may also be provided.

A method of forming fiducial marks to assist in the alignment of the pixelated structures on the cathode and anode planes has been described earlier and illustrated in the various parts of Figures 4 and 5. However, some residual misalignment may still occur. This is particularly troublesome in colour displays where misalignment in the direction parallel with the cathode address lines 810 may result in electrons striking the wrong phosphor patch with an associated loss in colour purity.

Figure 8a illustrates one method of making a display more tolerant of misalignment. In this arrangement the conducting layer on the anode plane is in three interdigitated segments 801, 802 and 803. Each segment has phosphors of one primary colour. Said segments are driven by independent power supplies 804, 805 and 806, each of which is switched on for one third of a frame. Electrons from the cathode plane 800 are now sequentially attracted to each colour phosphor in turn and follow trajectories 807, 808 and 809. Since the other two colour phosphors are not energised they cannot luminesce and the effects of misalignment are avoided. However, because of electrical breakdown between segments, this approach can only be used in low anode voltage systems. Such an approach has been described for tip-based displays by Clerc *(US Patent 5,225,820)*.

Figure 8b illustrates an alternative arrangement in which the display is rendered tolerant of misalignment 811 by forming focusing electrons to each phosphor patch 812 by means of an electrode of interdigitate or mesh form 813 at a less positive potential 815 than the main anode supply 814. Each phosphor patch now sits within a potential well that is sufficiently attractive to electrons 816 to compensate for modest misalignment of the pixelated structures on the cathode and anode. Such an approach has been described for tip-based displays by Tsai et al *(US Patent 5,508,584)*.

Whilst some examples of the invention have been described above in the context of a matrix addressed flat panel display, the methods and structures disclosed herein may be utilised across a wide variety of devices. In particular, a non-addressed or partially addressed electron source may be constructed and incorporated into other electron devices or displays. A focus grid structure such as previously described may be used to either focus or retard emitted electrons. If used in the retarding mode, the arrangement can,

especially when combined with a magnetic field normal to the emitter surface, provide a source of low energy electrons that can substitute for a thermionic cathode in some devices.

Figure 9 shows one example of a planar non-addressed emitter structure that may be used as an electron source in a wide variety of applications.

On an electrically insulating substrate 901 there is provided a conducting layer 902 and a broad-area field emitting layer 903. A perforated focus grid layer 904 serves to guide electrons though emitter cells 907 which are formed by apertures in insulating layer 905 and gate layer 906. Such a structure may be fabricated by any of the appropriate methods described in this specification.

In this non-addressed application the electrically insulating substrate may be replaced by an electrically conducting one (e.g. a metal) and the functions of substrate 901 and conducting layer 902 combined. A metal substrate enables welding and many other standard engineering joining techniques to be used.

The current from such a structure is controlled as follows. A device incorporating the illustrated emitter structure is used in conjunction with an electron accelerating anode (not shown in Figure 9) to collect the emitted current. A DC or pulsed power supply 909 connected to points 910 and 911 is adjusted such that in the "on" condition, a suitable positive extraction field, typically ~ 10 MV m^{-1} (10 V/μm), is applied to the areas of broad-area field emitter exposed at the base of the emitter cells 907 whereas, in the "off" condition, the applied electric field is less than the threshold value for field

emission. Naturally, the applied potential may be varied to produce a pulsed or AC emission current.

Devices that can utilise this invention may include: field electron emission and other display panels; high power pulse devices such as electron MASERS and gyrotrons; crossed-field microwave tubes such as CFAs; linear beam tubes such as klystrons; flash x-ray tubes; triggered spark gaps and related devices; broad area x-ray sources for sterilisation; vacuum gauges; ion thrusters for space vehicles; lamps; particle accelerators; ozonisers; and plasma reactors.

In this specification, the verb "comprise" has its normal dictionary meaning, to denote non-exclusive inclusion. That is, use of the word "comprise" (or any of its derivatives) to include one feature or more, does not exclude the possibility of also including further features.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. A method of manufacturing a field electron emission cathode, comprising the steps of:

   a. depositing on an insulating substrate by low resolution means, a sequence of a first conducting layer, a field emitting layer and a second conducting layer to form at least one cathode electrode;
   b. depositing on said cathode electrode by low resolution means, a sequence of an insulating layer and a third conducting layer, to form at least one gate electrode;
   c. coating the structure thus formed with a photoresist layer;
   d. exposing said photoresist layer by high resolution means to form at least one group of emitting cells, the or each said group being located in an area of overlap between one said cathode electrode and one said gate electrode;
   e. etching sequentially said conducting and insulating layers to expose said field emitting layer in said cells; and
   f. removing remaining areas of said photoresist layer.

2. A method according to claim 1, wherein said cathode is a cathode array, said cathode electrode and said gate electrode comprise respectively cathode addressing tracks and gate addressing tracks, which tracks are arranged in addressable rows and columns, and step d. includes forming a pattern of said groups of emitting cells.

3. A method according to claim 2, wherein at least one of or all of said cathode addressing tracks address(es) a plurality of rows or columns of cells.

4. A method according to claim 2 or 3, wherein said steps of exposing and etching include the formation of fiducial marks on the cathode array, to facilitate the subsequent alignment of the array with an anode or other component after manufacture of the array.

5. A method according to any of the preceding claims, comprising the step of forming at least one of said conducting layers by application of a liquid bright metal or by electroless plating.

6. A method according to any of the preceding claims, comprising the step of forming at least one of said conducting layers by a means other than vacuum evaporation or sputtering.

7. A method according to any of the preceding claims, wherein said field emitting layer comprises a layer of broad area field emitter material.

8. A method according to any of the preceding claims, comprising the further steps of depositing sequentially a second insulating layer and fourth conducting layer onto the cathode after completion of steps a. to f., to form a focus grid.

9. A method of manufacturing a field electron emission cathode, in accordance with claim 1 and substantially as hereinbefore described with reference to Figures 1a to 1e of the accompanying drawings.

10. A method of manufacturing a field electron emission cathode, substantially as hereinbefore described with reference to Figure 3, Figures 4a to 4f, Figures 5a to 5d, Figure 6a or Figure 6b of the accompanying drawings.

11. A field electron emission cathode which has been manufactured by a method according to any of the preceding claims.

12. A field emission device comprising an anode having electroluminescent phosphors and a cathode according to claim 11, wherein the cathode is a cathode array in accordance with claim 2 and is arranged to bombard said phosphors.

13. A field emission device according to claim 12, wherein said phosphors are arranged in groups of red, green and blue to form a colour display.

14. A field emission device according to claim 13, including anode driving means for energising said red, green and blue groups in turn.

15. A field emission device according to claim 12, 13 or 14, further comprising an electrode of interdigitate or mesh form which is interposed between said phosphors and is arranged to be driven at a potential less than that at which said phosphors are driven, thereby to form potential wells around the phosphors in order to attract electrons towards said phosphors and compensate for any misalignment between cathode and anode.

16. A field emission device according to any of claims 11 to 15, wherein said cathode is provided with a further control grid over said gate electrode, and a driving means for so driving said control grid as to retard electrons emitted by the cathode.

17. A field emission device according to claim 16, further comprising means for providing a magnetic field normal to the emitter surface.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 98/03142

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01J9/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 795 622 A (MOTOROLA INC) 17 September 1997 see figures 9-11 see column 11, line 13 - line 17 see column 14, line 13 - line 53 ---	1,11
Y	HOOLE A C F ET AL: "DIRECTLY PATTERNED LOW VOLTAGE PLANAR TUNGSTEN LATERAL FIELD EMISSION STRUCTURES" JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART B, vol. 11, no. 6, 1 November 1993, pages 2574-2578, XP000423379 see page 2574, column 2, paragraph 4 - page 2575, column 2, paragraph 1 see figure 2 --- -/--	1,11

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Noordman, F

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 685 869 A (MOTOROLA INC) 6 December 1995 see column 1, line 18 - line 22 see column 6, line 50 - column 7, line 26; figure 6 ---	1,11
A	WO 97 06549 A (TUCK RICHARD ALLAN ;LATHAM RODNEY VAUGHAN (GB); TAYLOR WILLIAM (GB) 20 February 1997 cited in the application see page 24, line 12 - page 25, line 18; figure 13 -----	1

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

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